AMENDMENTS TO THE CLAIMS

1. (Currently amended) A word length reduction circuit for quantizing ~~quantising~~ an N-bit input signal sample into an n-bit output signal sample; the circuit comprising:

an input for receiving the N-bit input signal samples;

a ~~quantiser~~ quantizer coupled to the input, and arranged to output an n-bit signal corresponding to the N-bit input sample signal;

an outer feedback loop comprising a loop filter coupled between the output of the ~~quantiser~~ quantizer and subtraction means coupled to the word length reduction circuit input ~~and~~ for subtracting a feedback signal from the input signal, the loop filter having an inner feedback loop coupled between the output and the input of the loop filter.

2. (Original) A circuit according to claim 1 wherein the loop filter comprises an integrator structure.

3. (Original) A circuit according to claim 1 wherein the loop filter is a sigma-delta loop filter.

4. (Currently amended) A circuit according to claim 1 wherein the ~~first~~ outer feedback loop is arranged to receive the least significant N-n bits of the ~~input signal sample~~ signal input to the quantizer.

5. (Original) A circuit according to claim 1 wherein the means for subtracting is an adder for coupling the outer feedback loop to the circuit input.

6. (Currently amended) A circuit according to claim 5 further comprising a second adder for coupling the outer feedback loop to the input of the loop filter, such that the ~~second feed-back~~ inner feedback loop signal is subtracted from the feed-back signal from the ~~quantiser~~ quantizer.

7. (Original) A circuit according to claim 1 wherein the loop filter coefficients are implemented using shifters.

8. (Currently amended) A circuit according to claim 1, the loop filter further comprising limiters to limit signal levels and scaling factors to ~~normalise~~ normalize signal dynamic ranges.

9. (Currently amended) A Converter for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulated (PWM) digital audio signal for amplification in a digital amplifier; the Converter comprising: a word length reduction circuit according to claim 1; a modulator for converting the PCM signals to PWM signals, the modulator coupled to the output of the ~~quantising~~ quantizing circuit.

10. (Currently amended) A Converter according to claim 9 further comprising a ~~Lineariser~~ Linearizer for receiving input signal samples and an output coupled to the input of the word length reduction circuit for providing ~~linearised~~ linearized signal samples.

11. (Currently amended) A Converter according to claim 10 wherein the ~~Lineariser~~ Linearizer comprises:

means for determining an intermediate sample between two adjacent input signal samples;

means for determining the polarity of the intermediate sample;

means for determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference waveform by applying one of two estimation algorithms dependent on the polarity of the intermediate sample;

means for outputting a ~~linearised~~ linearized signal sample having an amplitude corresponding to the determined crossing amplitude.

12. (Original) A Converter according to claim 11 wherein the intermediate sample determining means is an interpolator.

13. (Original) A Converter according to claim 12 wherein the interpolator is a filter with a zero interleaved input.

14. (Original) A Converter according to claim 11 wherein the estimation algorithms are linear or straight line approximations.

15. (Original) A Converter according to claim 14 wherein the means for determining an intermediate sample and the means for determining the signal amplitude are merged by implementing the estimation algorithms:

$$y = \begin{cases} b(1+c(1+c)) & if \quad b \geq 0 \\ b(1+a(1+a)) & otherwise \end{cases}$$

where:

$$a = \frac{w(n-1) - w(n-2)}{2}$$
$$b = w(n-1) - a/2$$
$$c = \frac{w(n) - w(n-2)}{4}$$

w(n) = input signal sample at sample time n

16. (Original) A Converter according to claim 11 wherein the signal amplitude determining means comprises implementing Taylor Series calculations.

17. (Original) A digital amplifier comprising a Word length Reduction circuit according to claim 1 or a Converter according to claim 9.

18. (Currently amended) A word length reduction method for ~~quantising~~ quantizing an N-bit input signal sample into an n-bit output signal sample; the method comprising:

receiving the N-bit input signal samples;

~~quantising~~ quantizing the input signal samples in order to output an n-bit signal corresponding to the N-bit input sample signal;

subtracting a feedback signal from the input signal, the feedback signal derived from the output of the ~~quantiser~~ quantizer, and filtering the feedback signal with a loop filter having an inner feedback loop coupled between the output and the input of the loop filter.

19. (Original) A method according to claim 18 wherein the loop filter comprises an integrator structure.

20. (Original) A method according to claim 18 wherein the loop filter is a sigma-delta loop filter.

21. (Currently amended) A method according to claim 18 wherein the feedback signal is derived from the least significant N-n bits of the ~~input signal sample~~ signal to be quantized.

22. (Original) A method for converting a pulse coded modulation (PCM) digital audio signal to a pulse width modulated (PWM) digital audio signal for amplification in a digital amplifier; the method comprising:

word length reducing an N-bit input signal sample into an n-bit output signal sample according to claim 18;

modulating said word length reduced PCM signals into PWM signals.

23. (Currently amended) A method according to claim 22 further comprising ~~linearising~~ linearizing said received input signal samples prior to said word length reduction.

24. (Currently amended) A method according to claim 23 wherein the ~~Linearising~~ Linearizing comprises:

determining an intermediate sample between two adjacent input signal samples;

determining the polarity of the intermediate sample;

determining at what signal amplitude an input signal waveform defined by said input samples and the intermediate sample crosses a reference waveform by applying one of two estimation algorithms dependent on the polarity of the intermediate sample;

outputting a ~~linearised~~ linearlized signal sample having an amplitude corresponding to the determined crossing amplitude.

25. (Original) A method according to claim 24 wherein the intermediate sample determining comprises interpolation.

26. (Original) A method according to claim 24 wherein the estimation algorithms are linear or straight line approximations.

27. (Currently amended) A method according to claim 26 wherein determining the intermediate sample and determining the signal amplitude are merged using the estimation algorithms:

$$y = \begin{cases} b(1+c(1+c)) & \textit{if} \quad b \geq 0 \\ b(1+a(1+a)) & \textit{otherwise} \end{cases}$$

where:

$$a = \frac{w(n-1) - w(n-2)}{2}$$
$$b = w(n-1) - a/2$$
$$c = \frac{w(n) - w(n-2)}{4}$$

w(n) = input signal sample at sample time n

28. (Original) A method according to claim 24 wherein the signal amplitude determining comprises a Taylor Series calculation.

29. (Original) A method of digitally amplifying an audio signal comprising a Word length Reducing method according to claim 18 or a method of Converting according to claim 22.

30. (Original) A carrier medium carrying processor readable code for controlling a processor to carry out the method of claim 18.

31. (Currently amended) A noise shaper circuit for reducing the word length of a digital audio amplifier, the circuit comprising a ~~quantiser~~ quantizer in a feedback loop with a loop filter, the circuit arranged such that the input signal is unfiltered and the noise transfer function is 1/(1+G(z)) where G(z) is the loop filter.